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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/483,101	01/14/2000	Kevin J McGrath	5500-54700	7937

7590 09/24/2002

Lawrence J Merkel
Conley Rose & Tayon PC
P O Box 398
Austin, TX 78767-0398

EXAMINER
LI, AIMEE J

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/483,101	MCGRATH ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3, 4, 5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-22 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Formal Drawings as received on April 14, 2000; IDS as received on May 19, 2000; IDS as received on December 5, 2000; IDS as received on December 20, 2000; and IDS as received on July 23, 2001.

Information Disclosure Statement

3. It is unclear whether the applicant would like the co-pending applications listed on the attorney's IDS form found in Paper No. 6: IDS received on December 5, 2000 and Paper No. 6: IDS, received on July 23, 2001, to be printed.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the method in claims 17-22 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

5. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686

F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

7. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

8. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 1-7 and 10 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2 of copending Application No. 09/483,636 (herein referred to as copending application) in view of Hammond et al., U.S. Patent No. 5,774,686 (herein referred to as Hammond) and in further view of Pentium® Processor Family Developer's Manual Volume 3: Architecture and Programming Manual by Intel ©1996 (herein referred to as Intel).

10. Referring to claim 1, the copending application has taught a processor comprising

a. a segment register configured to store a segment selector identifying a segment descriptor including a first operating mode indication (copending application claim 1)

b. a control register configured to store an enable indication (copending application claim 1)

c. wherein said processor is configured to establish an operating mode responsive to said enable indication and said first operating mode indication (copending application claim 1)

11. In regards to the copending application, it is generally accepted in the art that operating mode refers to the operand size and address size, and it does not matter what size the operand

and address sizes are. See *In re Rose* 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955) (herein referred to as *In re Rose*).

12. Copending application has not taught a second operating mode indication and wherein said processor is configured to establish an operating mode responsive to said second operating mode indication. Hammond has taught a processor comprising a second operating mode indication and wherein said processor is configured to establish an operating mode responsive to said second operating mode indication (Hammond column 6-7, lines 61-9 and column 7, lines 34-39). It would have been obvious to a person of ordinary skill in the art to incorporate Hammond's second operating mode indication and response to it, because the second operating mode indicator allows for more than two combinations and/or choices of modes to be made. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the second operating mode, as taught by Hammond, in the segment descriptor of copending application to allow more choices mode choices to be made.

13. In addition, copending application has not taught a segment descriptor including a second operating mode indication. Intel has taught a segment descriptor including an operating mode indication (Intel page 11-12, Figure 11-8 and page 11-13, item D bit/B bit). It would have been obvious to a person of ordinary skill in the art to include the second operating mode indication in a segment descriptor, because it allows the operating mode to automatically vary depending on which selector is active and would therefore be an advantage over a single global mode flag, which would have to use an instruction cycle to change the flag setting before the instructions in the other operating modes could be executed. Therefore it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate a segment

descriptor including a second operating mode indication in the invention of copending application to increase speed.

14. Referring to claim 2, copending application has taught a processor:

a. wherein said operating mode is a first operating mode if said enable indication is in an enabled state and said first operating mode indication is in a first state (copending application claim 1)

15. Copending application has not taught a processor wherein said operating mode is a second operating mode if said enable indication is in said enabled state, said first operating mode indication is in a second state, and said second operating mode indication is in said first state. Hammond has taught a processor wherein said operating mode is a second operating mode if said enable indication is in said enabled state, said first operating mode indication is in a second state, and said second operating mode indication is in said first state (Hammond column 6-7, lines 61-9 and column 7, lines 34-39). It would have been obvious to a person of ordinary skill in the art to select an operating mode as taught by Hammond, because it would allow the processor to select which architecture to use. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to choose a second operating mode if said enable indication is in said enabled state, said first operating mode indication is in a second state, and said second operating mode indication is in said first state to select architectures.

16. Referring to claim 3, copending application has not taught a processor wherein said second operating mode is one of a plurality of operating modes available if said enable indication is in said enabled state and said first operating mode indication is in said second state, and

wherein said one of said plurality of operating modes is selected in response to a state or said second operating mode indication. Hammond has taught a processor wherein said second operating mode is one of a plurality of operating modes available if said enable indication is in said enabled state and said first operating mode indication is in said second state, and wherein said one of said plurality of operating modes is selected in response to a state or said second operating mode indication (Hammond column 4, lines 46-48; column 6-7, lines 61-69; and Figure 2). It would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate a processor as taught by Hammond, because it allows for more operating modes to be chosen from. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the plurality of mode in the processor of Hammond in the invention of copending application to allow more operating mode choices.

17. Referring to claim 4, copending application does teach one of said plurality of operating modes is a 32 bit operating mode (copending application claim 1).

18. Referring to claim 5, copending application does not teach one of said plurality of operating modes is a 16 bit operating mode. Hammond does teach one of said plurality of operating modes is a 16 bit operating mode (Hammond column 4, lines 60-64 and column 6, lines 32-55). It would have been obvious to a person of ordinary skill in the art to incorporate the 16 bit operating mode as taught by Hammond, because it allows the processor to be compatible with programs made for the 8086 architecture. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate

the 16 bit operating mode, as taught by Hammond, in the invention of copending application to allow for backwards compatibility.

19. Referring to claim 6, copending application has taught said first operating mode includes a default address size which is greater than 32 bits (copending application claim 1).

20. Referring to claim 7, copending application has taught said default address size applies to virtual addresses generated by said processor (copending application claims 1 and 2).

21. Referring to claim 10, copending application has not taught a processor wherein if said enable indication is in a disabled state, said first operating mode indication is undefined. Hammond has taught a processor wherein if said enable indication is in a disabled state, said first operating mode indication is undefined (Hammond column 7, lines 12-21). It would have been obvious to a person of ordinary skill in the art to incorporate the processor details above, as taught by Hammond, because if the processor were to be compatible with older programs and systems, the flag being used to indicate the first operating mode would be undefined in the older systems. Therefore it would have been obvious to incorporate the details of a processor, which, if the enable indication is in a disabled state, the first operating mode indication is undefined to allow for backwards compatibility.

22. In addition, copending application has not taught a processor wherein said processor is configured to establish said operating mode responsive to said second operating mode indication. Intel has taught a processor wherein said processor is configured to establish an operating mode responsive to an operating mode indication (Intel page 11-12, Figure 11-8 and page 11-13, heading D bit/B bit). It would have been obvious to a person of ordinary skill in the art to incorporate the details of the processor above, because this would ensure an operating mode is

always established no matter the conditions. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate in a processor a configuration to establish an operating mode responsive to an operating mode indication to ensure an operating mode is always selected.

23. Claims 8 and 9 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-4 of copending Application No. 09/483,636 (herein referred to as copending application) in view of Hammond Hammond et al., U.S. Patent No. 5,774,686 (herein referred to as Hammond) and Pentium® Processor Family Developer's Manual Volume 3: Architecture and Programming Manual by Intel ©1996 (herein referred to as Intel) and in further view of Alpert et al., U.S. Patent No. 5,617,554 (herein referred to as Alpert).

24. Referring to claim 8, copending application and Hammond have not taught a processor wherein a virtual address is generated according to a segmentation mechanism employed by said processor. Alpert has taught a processor wherein a virtual address is generated according to a segmentation mechanism employed by said processor (Alpert column 1, lines 27-29). It would have been obvious to a person of ordinary skill in the art to generate a virtual address through segmentation, because segmentation allows for variable byte sizes and external programs based on previous processors that used segmentation, such as the Intel Pentium®, would require segmentation to function properly. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made wherein a virtual address is generated according to a segmentation mechanism employed by said processor, as taught by Alpert, in the invention of copending application for flexibility and backwards compatibility.

25. Referring to claim 9, copending application has taught a processor wherein said default address size further applies to physical addresses generated by said processor (copending application claims 1-4).

26. Claims 11-16 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-5 of copending Application No. 09/483,636 (herein referred to as copending application) in view of Pentium® Processor Family Developer's Manual Volume 3: Architecture and Programming Manual by Intel ©1996 (herein referred to as Intel).

27. Referring to claim 11, copending application has taught:

a. a control register configured to store an enable indication (copending application claim 1)

b. wherein said processor is configured to operate in an operating mode in which virtual addresses are greater than 32 bits responsive to said enable indication being in an enabled state and said operating mode indication being in a first state (copending application claims 1 and 2)

27. Copending application has not taught a segment register configured to store a segment selector and information from a segment descriptor, wherein said segment selector includes an index into a segment descriptor table stored in a memory to which said processor is coupled, said segment descriptor stored in said segment descriptor table in an entry indicated by said index, wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said segment selector, said segment descriptor including an operating mode indication. Intel has taught a segment register (Intel page 11-9, heading 11.2.1)

configured to store a segment selector (Intel page 11-9, Figure 11-6) and information from a segment descriptor (Intel page 11-9, Figure 11-6), wherein said segment selector includes an index into a segment descriptor table stored in a memory to which said processor is coupled (Intel page 11-10, Figure 11-7and paragraph 6), said segment descriptor stored in said segment descriptor table in an entry indicated by said index (Intel page 11-10, paragraph 6), wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said segment selector (Intel page 11-9, paragraph 2), said segment descriptor including an operating mode indication (Intel page 11-12, Figure 11-8 and page 11-13, item D bit/B bit). It would have been obvious to a person of ordinary skill in the art to incorporate the above by Intel, because this segmentation technique allows for variable byte sizes and external programs based on previous processors that used segmentation, such as the Intel Pentium®, would require segmentation to function properly. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the segmentation register, selector, descriptor, and tables above, as taught by Intel, in the invention of copending application for flexibility and backwards compatibility. In regards to the copending application, it is generally accepted that setting the operating mode establishes the size of the operand, and the exact operand size does not matter. See *In re Rose*.

28. Referring to claim 12, copending application has taught wherein physical addresses are greater than 32 bits in said operating mode (copending application claim 4). The actual size of the physical addresses does not matter. See *In re Rose*.

29. Referring to claim 13, copending application has taught wherein physical addresses are a first number of bits less than or equal to 64 bits (copending application claim 5). The actual size of the physical addresses does not matter. See *In re Rose*.

30. Referring to claim 14, copending application has taught wherein virtual addresses are a first number less than or equal to 64 bits (copending application claim 3). The actual size of the virtual addresses does not matter. See *In re Rose*.

31. Referring to claim 15, copending application has not taught wherein said segment descriptor further includes a privilege level. Intel has taught a segment descriptor includes a privilege level (Intel page 11-12, Figure 11-8 and page 11-15, paragraph 2). It would have been obvious to a person of ordinary skill in the art to incorporate the privilege level in the segment descriptor, as taught by Intel, because it controls access to the segment. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate a segment descriptor which includes a privilege level, as taught by Intel, in the invention of copending application to control access to the segment.

32. Referring to claim 16, copending application has not taught a processor further comprising a second control register configured to store a second enable indication, wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said second enable indication being in said enabled state. Intel has taught multiple control registers which allow modification of the state of the processor (Intel page 3-8, heading Registers), including the states of the segmentation unit (Intel page 10-6, Figure 10-3). It would have been obvious to a person of ordinary skill in the art to include another indication in a control register separate from the enable to signal when a segment descriptor will be read,

because it allows the user to control the state of the segmentation unit in the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate a second control register configured to store a second enable indication, wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said second enable indication being in said enabled state, as taught by Intel, in the invention of copending application to increase control over segmentation.

33. Claims 17-22 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 9-11 of copending Application No. 09/483,636 (herein referred to as copending application) in view of Hammond et al., U.S. Patent No. 5,774,686 (herein referred to as Hammond).

34. Referring to claim 17, copending application has taught a method:

a. establishing an operating mode in a processor in response to an enable indication in a control register within said processor, a first operating mode indication in a segment descriptor (copending application claim 9)

b. fretching operands and generating addresses in response to said operating mode (copending application claim 9)

35. Copending application has not taught a second operating mode indication in said segment descriptor. Hammond has taught a processor comprising a second operating mode indication (Hammond column 6-7, lines 61-9 and column 7, lines 34-39). It would have been obvious to a person of ordinary skill in the art to incorporate Hammond's second operating mode indication, because the second operating mode indicator allows for more than two combinations and/or

choices of modes to be chosen. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the second operating mode, as taught by Hammond, in the method of copending application to allow more modes to be chosen.

36. Referring to claim 18, copending application has taught a method wherein said establishing comprises establishing a first operating mode responsive to said enable indication being in an enabled state and said first operating mode indication being in a first state, and wherein said first operating mode includes a default address size greater than 32 bits (copending application claim 9). In regards to the copending application, it is generally accepted in the art that operating mode refers to the operand size and address size, and it does not matter what size the operand and address sizes are. See *In re Rose*.

37. Referring to claim 19, copending application has taught a method wherein said default address size applies to a virtual address (copending application claim 10).

38. Referring to claim 20, copending application has taught a method wherein said default address size applies to a physical address (copending application claim 11).

39. Referring to claim 21, copending application has taught a method wherein said first operating mode includes a default address size of 32 bits (copending application claim 9). Copending application has not taught a method wherein said establishing further comprises establishing a second operating mode responsive to said enable indication being in an enabled state, said first operating mode indication being in a second state, and said second operating mode being in said first state. Hammond has taught establishing a second operating mode responsive to said enable indication being in an enabled state, said first operating mode indication being in a second state, and said second operating mode being in said first state

(Hammond column 4, lines 60-64; column 6, lines 52-55; and columns 6-7, lines 61-9). It would have been obvious to a person of ordinary skill in the art to establish a second operating mode as taught by Hammond, because it would allow the processor to run multiple different types of instruction and address architectures. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to establish a second operating mode as taught by Hammond in the invention of copending application to increase compatibility with other architectures.

40. Referring to claim 22, copending application has not taught establishing one of a plurality of operating modes if said enable indication is in said enabled state and said first operating mode indication is in a second state, and wherein said one of said plurality of operating modes is selected in response to a state of said second operating mode indication. Hammond has taught establishing one of a plurality of operating modes if said enable indication is in said enabled state and said first operating mode indication is in a second state, and wherein said one of said plurality of operating modes is selected in response to a state of said second operating mode indication (Hammond column 4, lines 46-48; columns 6-7, lines 61-9; and Figure 2). It would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate a processor as taught by Hammond, because it allows for more operating modes to be chosen from. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the plurality of mode in the processor of Hammond in the invention of copending application to allow more operating mode choices.

41. These are provisional obviousness-type double patenting rejections.

Claim Rejections - 35 USC § 103

42. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

43. Claims 1-7, 10, 11, 14, 15, 17-19, 21, and 22 rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond in view of Intel.

44. Referring to claim 1, Hammond has taught:

a. a control register configured to store an enable indication, wherein said processor is configured to establish an operating mode responsive to said enable indication, said first operating mode indication, and said second operating mode indication (Hammond columns 6-7, lines 61-9 and column 7, lines 34-39)

45. Hammond has not taught a segment register configured to store a segment selector identifying a segment descriptor including a first operating mode indication and a second operating mode indication. However, Hammond does teach including a segmentation unit (Hammond column 4, lines 54-57) compatible with the x86 structure and a second operating mode indication stored in the control register (Hammond column 6-7, lines 61-9 and column 7, lines 34-39). Intel, which is based on the x86 structure and instruction set (Intel page 2-1, paragraphs 1-2), has taught that it is common to have a segment register configured to store a segment selector identifying a segment descriptor including operating mode indication (Intel page 11-9, Figure 11-6; page 11-10, paragraph 4; page 11-12, Figure 11-8; and page 11-13, item D bit/B bit). It would have been obvious to a person of ordinary skill in the art that the

segmentation unit in Hammond represented the segment register, segment selector, and segment descriptor taught by Intel and to move the operating mode indicators to the segmentation unit, because the segment register, selector, and descriptor are components found in a generic x86 compatible segmentation unit and moving the operating mode indicators to the segment descriptor would allow the operating mode to automatically vary depending on which selector is active and would be an advantage over a single global mode flag, which would have to use an instruction cycle to change the flag setting before the instructions in the other operating modes could be executed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate a segment register configured to store a segment selector identifying a segment descriptor including a first operating mode indication and a second operating mode indication, as taught by Intel, in the invention of Hammond for backwards compatibility and to increase speed.

46. Referring to claim 2, Hammond has taught a processor wherein said operating mode is a first operating mode if said enable indication is in an enabled state and said first operating mode indication is in a first state, and wherein said operating mode is a second operating mode if said enable indication is in said enabled state, said first operating mode indication is in a second state, and said second operating mode indication is in said first state (Hammond columns 6-7, lines 61-69 and column 7, lines 34-39).

47. Referring to claim 3, Hammond has taught a processor wherein said second operating mode is one of a plurality of operating modes available if said enable indication is in said enabled state and said first operating mode indication is in said second state, and wherein said one of said plurality of operating modes is selected in response to a state of said second operating

mode indication (Hammond column 4, lines 46-48; column 6-7, lines 61-9; column 7, lines 34-39; and Figure 2).

48. Referring to claim 4, Hammond has taught a processor wherein one of said plurality of operating modes is a 32 bit operating mode (Hammond column 4, lines 60-64 and column 6, lines 52-55).

49. Referring to claim 5, Hammond has taught a processor wherein one of said plurality of operating modes is a 16 bit operating mode (Hammond column 4, lines 60-64 and column 6, lines 52-55).

50. Referring to claim 6, Hammond has taught a processor wherein said first operating mode includes a default address size which is greater than 32 bits (Hammond column 5, 12-13 and column 6, lines 52-55).

51. Referring to claim 7, Hammond has taught a processor wherein said default address size applies to virtual addresses generated by said processor (Hammond column 5, lines 12-13 and column 6, lines 52-55).

52. Referring to claim 10, Hammond has taught a processor

a. wherein if said enable indication is in a disabled state, said first operating mode indication is undefined (Hammond column 7, lines 12-21).

53. Hammond has not taught a processor wherein said processor is configured to establish said operating mode responsive to said second operating mode indication. Intel has taught a processor wherein said processor is configured to establish an operating mode responsive to an operating mode indication (Intel page 11-12, Figure 11-8 and page 11-13, heading D bit/B bit). It would have been obvious to a person of ordinary skill in the art to incorporate the details of the

processor above, because this would ensure an operating mode is always established no matter the conditions. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate in a processor a configuration to establish an operating mode responsive to an operating mode indication to ensure an operating mode is always selected.

54. Referring to claim 11, Hammond has taught a processor:

a. a control register configured to store an enable indication (Hammond columns 6-7, lines 61-69 and column 7, lines 34-39)

b. wherein said processor is configured to operate in an operating mode in which virtual addresses are greater than 32 bits responsive to said enable indication being in an enabled state and said operating mode indication being in a first state (Hammond column 5, lines 12-13; column 6, lines 52-55; columns 6-7, lines 61-9; and column 7, lines 34-39)

55. Hammond has not taught a segment register configured to store a segment selector and information from a segment descriptor, wherein said segment selector includes an index into a segment descriptor table stored in a memory to which said processor is coupled, said segment descriptor stored in said segment descriptor table in an entry indicated by said index, wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said segment selector, said segment descriptor including an operating mode indication. However, Hammond does teach including a segmentation unit (Hammond column 4, lines 54-57) compatible with the x86 structure. Intel, which is based on the x86 structure and instruction set (Intel page 2-1, paragraphs 1-2), has taught a segment register (Intel page 11-9,

heading 11.2.1) configured to store a segment selector (Intel page 11-9, Figure 11-6) and information from a segment descriptor (Intel page 11-9, Figure 11-6), wherein said segment selector includes an index into a segment descriptor table stored in a memory to which said processor is coupled (Intel page 11-10, Figure 11-7and paragraph 6), said segment descriptor stored in said segment descriptor table in an entry indicated by said index (Intel page 11-10, paragraph 6), wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said segment selector (Intel page 11-9, paragraph 2), said segment descriptor including an operating mode indication (Intel page 11-12, Figure 11-8 and page 11-13, item D bit/B bit). It would have been obvious to a person of ordinary skill in the art to incorporate the above by Intel, because this is a standard segmentation technique and is based on the x86 structure, which would ensure compatibility. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made that the segmentation unit in Hammond includes a segment register configured to store a segment selector and information from a segment descriptor, wherein said segment selector includes an index into a segment descriptor table stored in a memory to which said processor is coupled, said segment descriptor stored in said segment descriptor table in an entry indicated by said index, wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said segment selector, said segment descriptor including an operating mode indication, as taught by Intel.

56. Referring to claim 14, Hammond has taught a processor wherein virtual addresses are a first number of bits less than or equal to 64 bits (Hammond column 5, lines 17-18).

57. Referring to claim 15, Hammond has not taught wherein said segment descriptor further includes a privilege level. Intel has taught wherein said segment descriptor further includes a privilege level (Intel 11-12, Figure 11-8 and page 11-15, paragraph 2). It would have been obvious to a person of ordinary skill in the art would have included the privilege level in said segment descriptor, because it would control access to the segment. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made that said segment descriptor further includes a privilege level, as taught by Intel, in the invention of Hammond to control access to the segment.

58. Referring to claim 16, Hammond has not taught a processor further comprising a second control register configured to store a second enable indication, wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said second enable indication being in said enabled state. Intel has taught multiple control registers which allow modification of the state of the processor (Intel page 3-8, heading Registers), including the states of the segmentation unit (Intel page 10-6, Figure 10-3). It would have been obvious to a person of ordinary skill in the art to include another indication in a control register separate from the enable to signal when a segment descriptor will be read, because it allows the user to control the state of the segmentation unit in the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate a second control register configured to store a second enable indication, wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said second enable indication being in said enabled state, as taught by Intel, in the invention of Hammond to increase control over segmentation.

59. Referring to claim 17, Hammond has taught a method:

a. establishing an operating mode in a processor in response to an enable indication in a control register within said processor, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor (Hammond columns 6-7, lines 61-9 and column 7, lines 34-39)

60. Hammond has not explicitly taught fetching operands and generating addresses in response to said operating mode. Intel has explicitly taught fetching operands and generating addresses in response to said operating mode (Intel page 11-12, Figure 11-8 and page 11-13, item D bit/B bit). It would have been obvious to fetch operands and generate addresses in response to the operating mode, because when changing operating mode, the address size and operand size changes and the new sizes are required for the device to function properly. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to fetch operands and generate addresses in response to said operating mode, as taught by Intel, in the invention of Hammond to ensure the processor functions properly.

61. Referring to claim 18, Hammond has taught a method wherein said establishing comprises establishing a first operating mode responsive to said enable indication being in an enabled state and said first operating mode indication being in a first state, and wherein said first operating mode includes a default address size greater than 32 bits (Hammond column 5, lines 12-13; column 6, lines 52-55; columns 6-7, lines 61-9; and column 7, lines 34-39).

62. Referring to claim 19, Hammond has taught a method wherein said default address size applies to a virtual address (Hammond column 5, lines 12-13 and column 6, lines 52-55).

63. Referring to claim 21, Hammond has taught a method wherein said establishing further comprises establishing a second operating mode responsive to said enable indication being in an enabled state, said first operating mode indication being in a second state, and said second operating mode being in said first state, and wherein said first operating mode includes a default address size of 32 bits (Hammond columns 6-7, lines 61-9; column 4, lines 60-64; and column 6, lines 52-55).

64. Referring to claim 22, Hammond has taught a method whereing said establishing further comprises establishing one of a plurality of operating modes if said enable indication is in said enabled state and said first operating mode indication is in a second state, and wherein said one of said plurality of operating modes is selected in response to a state of said second operating mode indication (Hammond column 4, lines 46-49; column 6-7, lines 61-9; and Figure 2).

65. Claims 8, 9, 12, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond in view of Intel as applied to claims 1-7 above, and further in view of Alpert.

66. Referring to claim 8, Hammond in view of Intel has not taught a virtual address is generated according to a segmentation mechanism employed by said processor. However, Hammond does teach a virtual address was generated and includes a segmentation unit. Alpert has taught virtual memory, typically, is generated using techniques such as segmentation, paging, or a combination of both (Alpert column 1, lines 27-29). It would have been obvious to a person of ordinary skill in the art to use segmentation to generate a virtual address, because segmentation allows for variable byte sizes and external programs based on previous processors that used segmentation, such as the Intel Pentium®, would require segmentation to function properly. Therefore, it would have been obvious to a person of ordinary skill in the art at the

time this invention was made that a virtual address is generated according to a segmentation mechanism employed by said processor for flexibility and backwards compatibility.

67. Referring to claim 9, Hammond in view of Intel has not taught a processor wherein said default address size further applies to physical addresses generated by said processor. Alpert has taught a physical memory size greater than 32 bits (Alpert Abstract, lines 3-6), which is the default address size. It would have been obvious to a person of ordinary skill in the art to apply the default address size of greater than 32 bits to the physical address, as taught by Alpert, because it increases the physical memory size. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made that said default address size further applies to physical addresses generated by said processor, as taught by Alpert, in the invention of Hammond to increase the physical memory size.

68. Referring to claim 12, Hammond in view of Intel has not taught a processor wherein physical addresses are greater than 32 bits in said operating mode. Alpert has taught a physical memory size greater than 32 bits (Alpert Abstract, lines 3-6), which is the default address size. It would have been obvious to a person of ordinary skill in the art to apply the default address size of greater than 32 bits to the physical address, as taught by Alpert, because it increases the physical memory size. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made that said default address size further applies to physical addresses generated by said processor, as taught by Alpert, in the invention of Hammond to increase the physical memory size.

69. Referring to claim 13, Hammond in view of Intel has not taught wherein physical addresses are a first number of bits less than or equal to 64 bits. Alpert has taught wherein

physical addresses are a first number of bits less than or equal to 64 bits (Alpert column 3, lines 14-26, 35-38, and lines 44-48 and column 4, lines 32-39). It would have been obvious to a person of ordinary skill in the art to apply physical addresses that are a first number of bits less than or equal to 64 bits, as taught by Alpert, because it increases the physical memory size but maintains compatibility with previous smaller address size architectures and the IEEE standard. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made that physical addresses are a first number of bits less than or equal to 64 bits, as taught by Alpert, in the invention of Hammond to increase the physical memory size and maintain compatibility.

70. Referring to claim 20, Hammond in view of Intel has not taught a method wherein said default address size applies to a physical address. Alpert has taught a physical memory size greater than 32 bits (Alpert Abstract, lines 3-6), which is the default address size. It would have been obvious to a person of ordinary skill in the art to apply the default address size of greater than 32 bits to the physical address, as taught by Alpert, because it increases the physical memory size. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made that said default address size further applies to physical addresses generated by said processor, as taught by Alpert, in the invention of Hammond to increase the physical memory size.

Conclusion

71. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by

the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Grochowski et al., U.S. Patent Number 5,692,167, has taught a processor with a segment selector containing a default mode indicator and a control register containing another default indicator.

b. Richter et al., U.S.Patent Number 5,481,684, has taught segment and control registers.

c. Baum et al., U.S. Patent Number 5,381,537, has taught an addressing system in 32 or 64 bits.

d. Advanced 80386 Programming Techniques by James L. Turley ©1988 has taught segment and control registers with indicator bits and an instruction prefix modifying the address size.

e. Pentium Processor Family Developer's Manual by Intel ©1997 has taught segment and control registers with indicator bits and instruction prefixes modifying address and operand sizes.

f. Intel Architecture Software Developer's Manual Volume 2: Instruction set Reference by Intel ©1997 has taught segment and control registers with indicator bits and instruction prefixes modifying address and operand sizes.

72. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-F 7:30am-4:00pm.
73. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.
74. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

September 18, 2002

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100